BCA-107: LOGICAL ORGANIZATION OF COMPUTER-II

External Marks: 80
Internal Marks: 20

Time: 3 hours

Note: Examiner will be required to set NINE questions in all. Question Number 1 will consist of total 8 parts (short-answer type questions) covering the entire syllabus and will carry 16 marks. In addition to the compulsory question there will be four units i.e. Unit-I to Unit-IV. Examiner will set two questions from each Unit of the syllabus and each question will carry 16 marks. Student will be required to attempt FIVE questions in all. Question Number 1 will be compulsory. In addition to compulsory question, student will have to attempt four more questions selecting one question from each Unit.

UNIT - I

Sequential Logic: Characteristics, Flip-Flops, Clocked RS, D type, JK, T type and Master-Slave flip-flops. State table, state diagram and state equations. Flip-flop excitation tables

UNIT - II

Sequential Circuits: Designing registers – Serial Input Serial Output (SISO), Serial Input Parallel Output (SIPO), Parallel Input Serial Output (PISO), Parallel Input Parallel Output (PIPO) and shift registers. Designing counters – Asynchronous and Synchronous Binary Counters, Modulo-N Counters and Up-Down Counters

UNIT - III

Memory & I/O Devices: Memory Parameters, Semiconductor RAM, ROM, Magnetic and Optical Storage devices, Flash memory, I/O Devices and their controllers.

UNIT - IV

Instruction Design & I/O Organization: Machine instruction, Instruction set selection, Instruction cycle, Instruction Format and Addressing Modes. I/O Interface, Interrupt structure, Program-controlled, Interrupt-controlled & DMA transfer, I/O Channels, IOP.

SUGGESTED READINGS

1. Gill, Nasib Singh and Dixit J.B.: Digital Design and Computer Organisation, University Science Press (Laxmi Publications), New Delhi.
2. M. Morris Mano, Digital Logic and Computer Design, Prentice Hall of India Pvt. Ltd.
3. V. Rajaraman, T. Radhakrishnan, An Introduction to Digital Computer Design, Prentice Hall of India Pvt. Ltd.
4. Andrew S. Tanenbaum, Structured Computer Organization, Prentice Hall of India Pvt. Ltd.
5. Nicholas Carter, Schaum's Outlines Computer Architecture, Tata McGraw Hill.

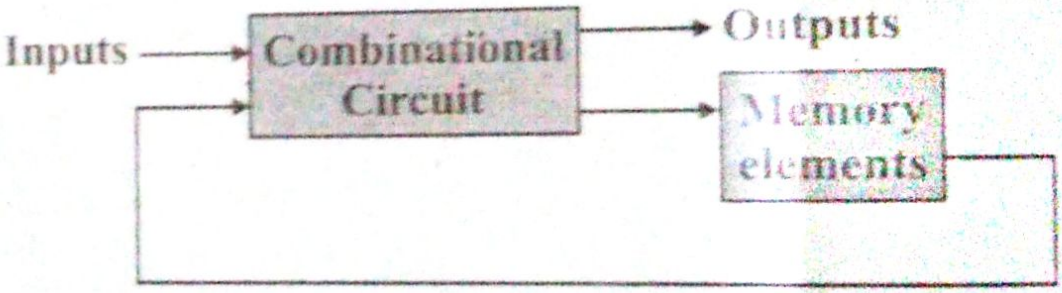
Note: Latest and additional good books may be suggested and added from time to time.

Q2.(b) What do you mean by sequential circuit? What are its characteristics? Also explain types of sequential circuit.

Ans. Sequential Circuit

The sequential circuit is a circuit whose output depends on the present input as well as on past outputs.

Sequential circuit is a digital circuit whose logic states depend on a specified time sequence. A sequential circuit consists of a combinational circuit to which memory elements are connected to form a feedback path.



It is clear from the diagram that sequential circuit consists of combinational circuit which:

- ***Accepts signals from external inputs and output of memory elements***
- ***Generates signals for external outputs and for inputs to memory elements.***

Characteristics of Sequential circuits

Characteristics of sequential circuits are:

1. *It is a circuit which works in sequence by taking present inputs and past value of inputs.*
2. *It contains at least one memory element for storage of previous outputs.*
3. *In this output is fed as input directly or indirectly.*
4. *It becomes complex to design due to presence memory element.*
5. *Its performance is described by the set of subsequent state values as well as set of output values.*
6. *It is comparatively slower in speed as output is delayed.*
7. *It requires less hardware for its realization.*
8. *It is cheaper in cost because of less hardware requirement.*

Types of Sequential circuits

The sequential circuits are classified on the basis of timing of their signals. These are of the following two types:

1. Synchronous sequential circuit
2. Asynchronous sequential circuit

1. Synchronous sequential circuit

A synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signal at discrete instants of time.

In these circuits:

- *Events take place during regular timing pluses.*
- *Memory elements are clocked flip flops.*
- *The change in input signals can affect memory element on activation of clock signal.*

2. Asynchronous sequential circuit

An asynchronous sequential circuit is a system whose behavior depends upon the sequence in which the input signals change.

In these circuits:

- *Events do not have to wait for the timing pulses. They can occur only after previous event is over or completed.*
- *Memory elements are either unclocked flip flops or time delay elements.*
- *The change in input signals can affect memory element at any instant of time.*

Q2.(a) What are flip flops? What are its general characteristics? Also write the applications of flip flops.

Ans. Flip flop

A flip flop is a circuit capable of storing one bit of information either 1 or 0 based on inputs applied on it. It is a data storage system used to store information in sequential logic systems.

A flip flop has two stable states. One of the stable states is SET or 1 and the other stable state is called RESET, CLEAR or 0. There are two input lines, two output lines and a clock line. The state of the output at any instant of time depends upon the past outputs and the data input present at that instant of time.

Flip flops are combined to form counters, shift registers and various memory devices.

Characteristics of flip flops

There are many types of flip flops but all share the following characteristics:

- ***A flip flop is a basic memory element.***
- ***A flip flop is a bi-stable multivibrator.***
- ***A flip flop circuit has two stable states. One is SET or 1 and the other stable state is called RESET, CLEAR or 0.***
- ***It continues to remain in either of the states until some triggering signal is applied to change its state.***

- *A flip flop can have one or more inputs. These inputs cause the flip flop to switch back and forth between its possible output states.*
- *The two output signals Q and $\overline{Q}$ are always complementary to each other i.e. if Q = 1 then $\overline{Q}$ = 0 and if Q = 0 then $\overline{Q}$ = 1.*
- *It serves as a storage device. It stores 1 when its Q output is a 1 and stores a 0 when its Q output is a 0.*

Applications of flip flops

There are a number of applications of flip flops. Some of them are listed below:

1. Transfer of data
2. Digital counting
3. Basic building block
4. Frequency division
5. Data storage

1. Transfer of data

The data stored in one flip flop can be easily transferred to another flip flop. The data can be transferred in a serial fashion i.e. bit by bit or in parallel form i.e. all bits at a time from the Q outputs of each of the flip flops.

2. Digital counting

A number of flip flops can be connected in a manner to count the pulses electronically. A single flip flop can count upto 2 pulses; two flip flops can count upto $2^2 = 4$

pulses. Similarly, n flip flops can count upto 2^n pulses. Flip flops can be used to count up or down or up/down.

3. Basic building block

A flip flop is used as a basic building block in sequential circuits such as counters and registers.

4. Frequency division

Flip flops are used for frequency division. One flip flop can divide the frequency to half.

5. Data storage

Data storage is the basic feature of digital system. Flip flops are used for parallel as well as serial data storage.

Q3.(b) Explain clocked RS flip flop.

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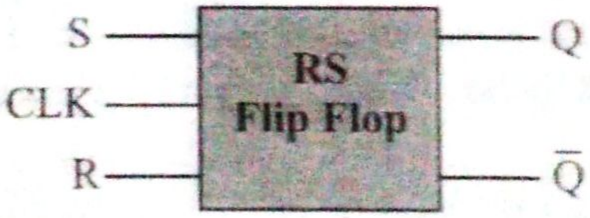
Ans. Clocked RS flip flop

If a clock input is added to an ordinary RS flip flop then a clocked flip flop with synchronous operation is achieved. This action is called synchronous because the data can only be sent to reset or set the flip flop when the clock signal is high.

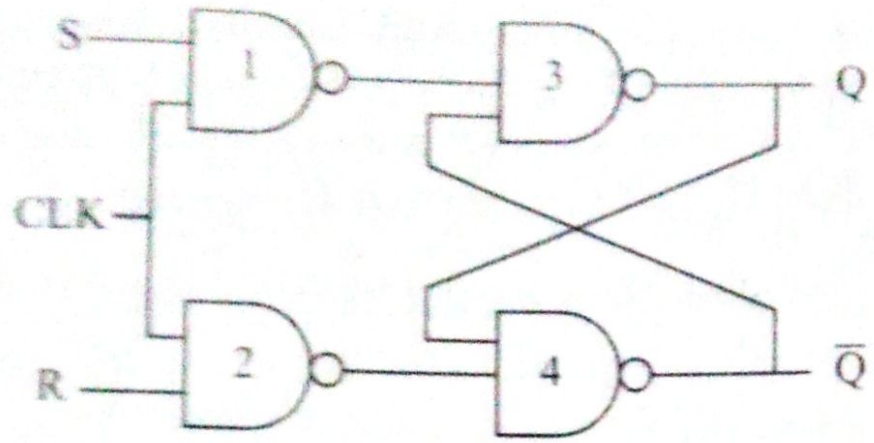
The synchronous operation is very important because it is required to control the operation of digital systems from a central clock pulse generator and also to avoid any time delay within counters or registers.

This method of connecting the clock signal is called positive edge triggered because NAND gates 1 and 2 will be open to R or S data only when the clock goes positive.



(Logic symbol for Clocked RS flip flop)

The circuit diagram of Clocked RS flip flop is shown below:



(Logic diagram for Clocked RS flip flop)

It is clear from the above diagram that two NAND gates 1 and 2 are added to the RS flip flop to convert it into clocked RS flip flop.

Truth table of Clocked RS flip flop is shown below:

CLK	S	R	Q_{n+1}	Comment
0	X	X	Q_n	No Change
1	0	0	Q_n	No Change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	---	Invalid

Working

1. If CLK (clock pulse) is absent i.e. if CLK = 0 then the output of NAND gates 1 and 2 are 1 irrespective of the values of S and R. This means there is no change.

2. If S = 0 and R = 0 with CLK going high i.e. CLK = 1 then output of flip flop at (n+1)th clock pulse is same as the previous clock pulse i.e. at nth clock pulse. Thus $Q_{n+1} = Q_n$ means there is no change.

3. If S = 0 and R = 1 with CLK going high i.e. CLK = 1 then Q_{n+1} is equal to 0. This means flip flop is in reset state.

4. If S = 1 and R = 0 with CLK going high i.e. CLK = 1 then Q_{n+1} is equal to 1 irrespective of the value at nth clock pulse. This means flip flop is in set state.

5. If S = 1 and R = 1 with CLK going high i.e. CLK = 1 then the next state of the circuit is indeterminate and an invalid or race condition is said to have occurred and so it should be avoided.

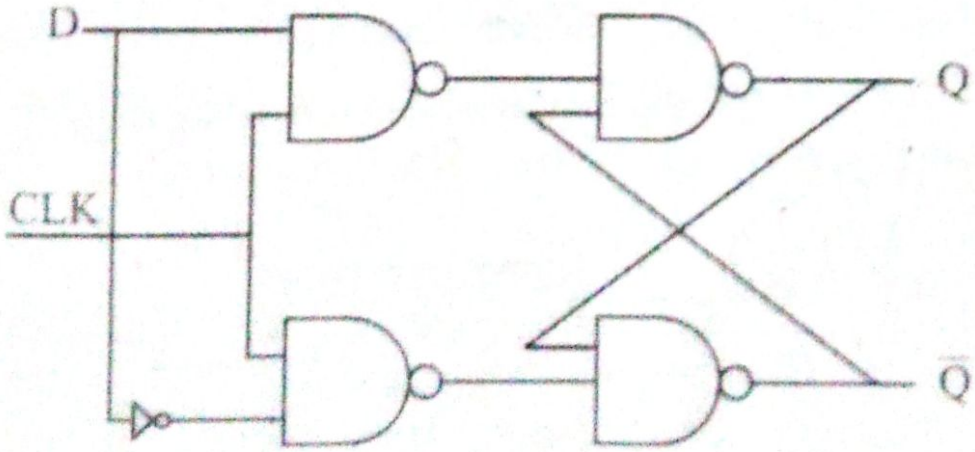
Q3.(c) Explain the working of D type flip flop with logic diagram. **MDU BCA 2011**

Ans. D flip flop

A D flip flop is the modified form of SR flip flop. The D flip flop stands for delay flip flop. It is useful for temporary data storage. It eliminates an invalid or race condition which comes across in the RS flip flop. D flip flop was developed to fulfill the need of single data input.

(Logic symbol for clocked D flip flop)

The circuit diagram of D flip flop is shown below:



(Logic diagram for clocked D flip flop)

When clock is absent, the circuit gets disabled i.e. when CLK is off (zero) then whatever be the D the output will no change.

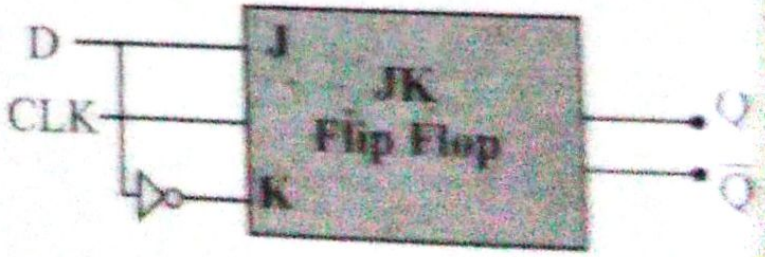
When clock is present i.e. input is high, the circuit works and input D is transferred to the output Q at the end of clock pulse hence output is delayed. Thus this flip flop is called delayed flip flop.

Truth table of D flip flop is shown below:

CLK	D	Q_{n+1}	Comment
0	0	0	No Change
0	1	1	
1	0	0	Reset
1	1	1	Set

SR or JK flip flop can be converted to D flip flop as shown below:

(SR flip flop converted into D flip flop)



(JK flip flop converted into D flip flop)

Q4.(a) Explain the operation of a JK Flip-Flop with a neat logic circuit and truth table.

IGU BCA 2018

OR

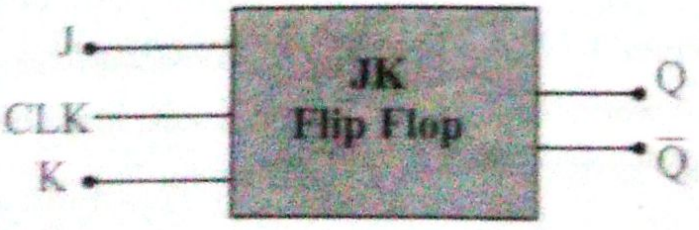
What is JK flip flop? Describe race around condition and explain how it can be removed in a Master-Slave flip flop. **MDU BCA 2010**

OR

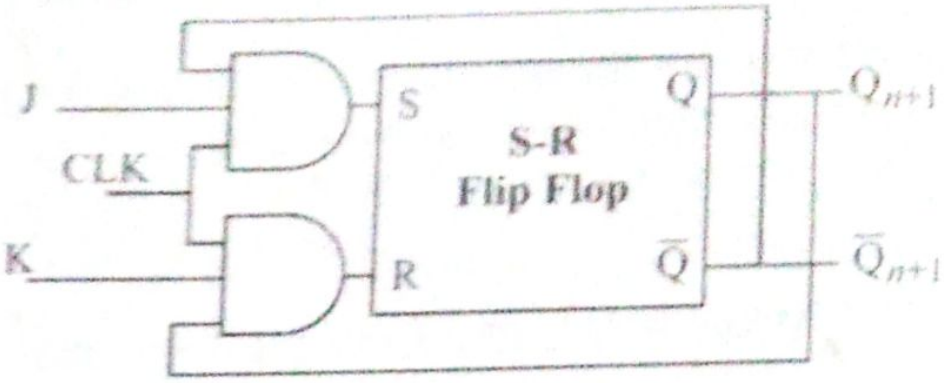
Explain working of a J-K flip flop. How race around condition is eliminated in this case.

Ans. J-K flip flop

J-K flip flop is the improved version of SR flip flop. The uncertainty state of an SR flip flop when S=R=1 can be eliminated by converting it to JK flip flop. In RS flip flop when both the inputs R and S were 1, then the output was invalid. JK flip flop is the improved version of SR flip flop so that when both inputs are 1 then the outputs Q and $\overline{Q}$ are complement of each other. The circuit diagram and truth table of J-K flip flop is shown below:



(Block diagram of J-K Flip Flop)



(Logic diagram of J-K Flip Flop)

CLK	J	K	Q_{n+1}	Description
1	0	0	Q_{n+1}	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q}_n$	Toggle

The J-K flip flop can be obtained from SR flip flop by ANDing J and K inputs with $\overline{Q}$ and Q respectively to obtain S and R inputs.

$$S = J.\overline{Q}$$

$$R = K.Q$$

Working of J-K flip flop

When CLK is absent i.e. CLK=0, the circuit does not responds to inputs. When CLK is present i.e. CLK=1, the circuit will work as follows:

- ***When J=0, K=0 i.e. both inputs are low then both AND gates are disabled irrespective of inputs and clock pulses. Thus there is no change in the state.***

- ***When J=0, K=1 i.e. J is a low and K is a high then the upper AND gate is disabled and lower AND gate responds to inputs leading to the Reset state***

- ***When J=1, K=0, the lower AND gate is disabled and the upper AND gate gets enabled. So, there is no way to reset the flip flop. Thus flip flop is in set state.***

- ***When both J and K are equal to 1 then the value of Q and $\overline{Q}$ will determine that whether the flip flop will be in set state or in reset state. If Q is high then the flip flop will be in reset state and when Q is low then it is in set state. This means flip flop will toggle when both J and K are equal to 1.***

Race Around condition

We know that in JK flip flop when J=1, K=1 & CLK=1, output toggles.

Suppose T_d = Propagation delay of flip flop

and T_p = Pulse time

If $T_p >> T_d$, the flip flop will toggle again and again at J=1, K=1 and CLK = 1 till CLK goes low making final output uncertain. This situation in JK flip flop is called race around condition.

A method to overcome the race around condition is JK Master Slave flip flop.

In JK Master Slave flip flop two flip flops are used. One is Master and the other is Slave. They are joined in

Q5.(b) Explain T Flip-Flop. MDU BCA 2017

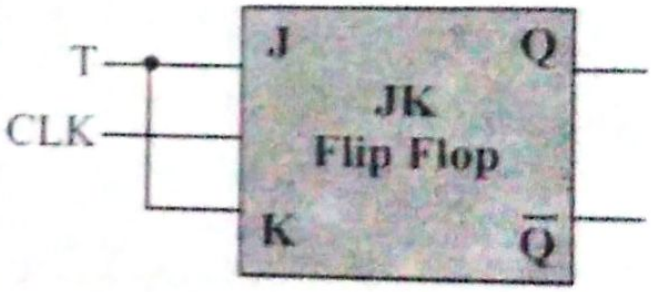
OR

Explain the working of T type flip flop with logic diagram.

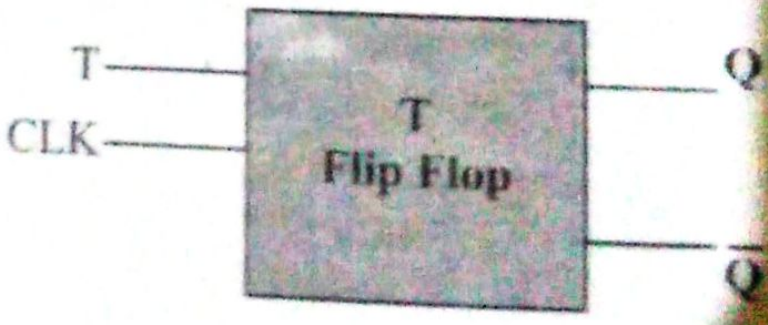
Ans. T type flip flop

In a J-K flip-flop, if both J and K are tied to same input, then the derived Flip-flop becomes T Flip-Flop.

This is a much simpler version of the J-K flip flop. Both the J and K inputs are connected together and thus are also called a single input J-K flip flop.

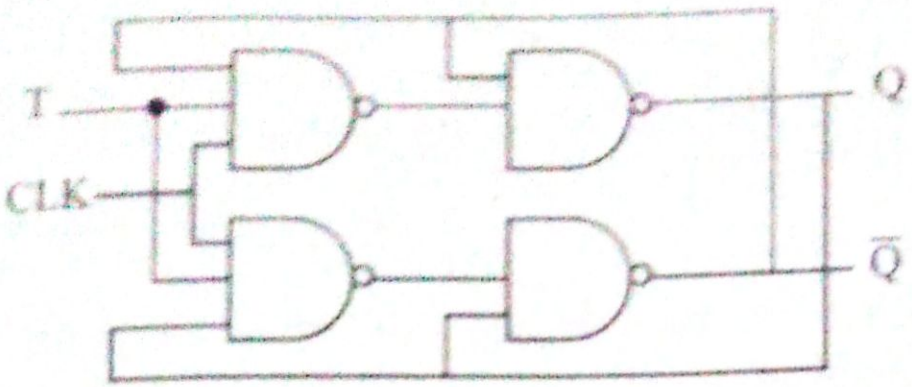


(T flip flop using J-K flip flop)



(Logic symbol for T flip flop)

The circuit diagram T flip flop is shown below:



(Logic diagram of T Flip Flop)

Truth table of T flip flop is shown below:

Inputs		Outputs	
CLK	**T**	Q_{n+1}	**Comment**
1	**0**	Q_n	**No Change**
1	**1**	$\bar{Q}_n$	**Toggle**

When T = 1 i.e. when T is high then output value Q_{n+1} is complement of the output Q_n. Thus, value of output toggles whenever T input is high.

Q4.(b) Explain Master-Slave Flip-Flop.

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OR

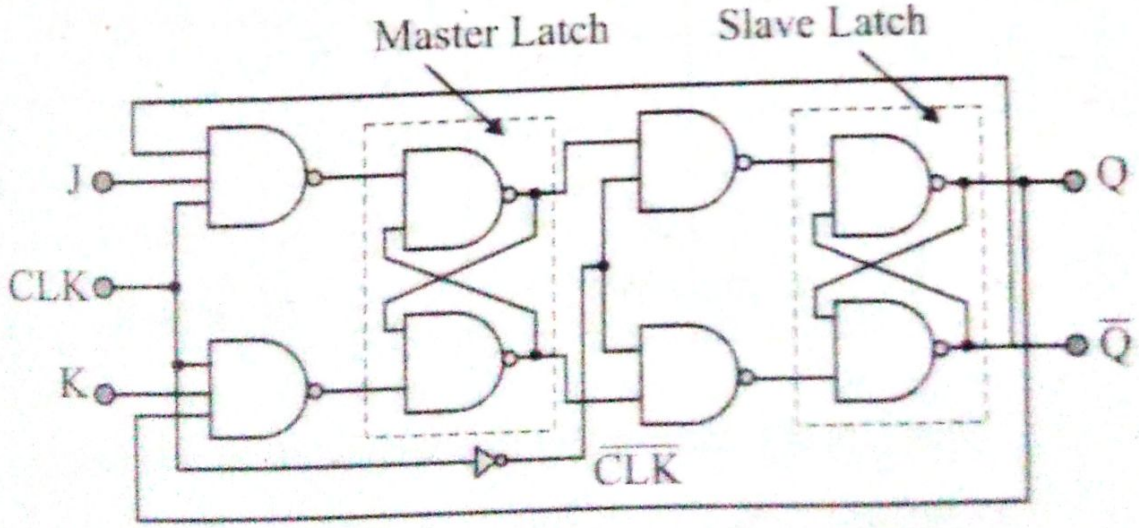
Explain Master–Slave J-K flip flop.

MDU BCA 2012

Ans. Master Slave J-K flip flop

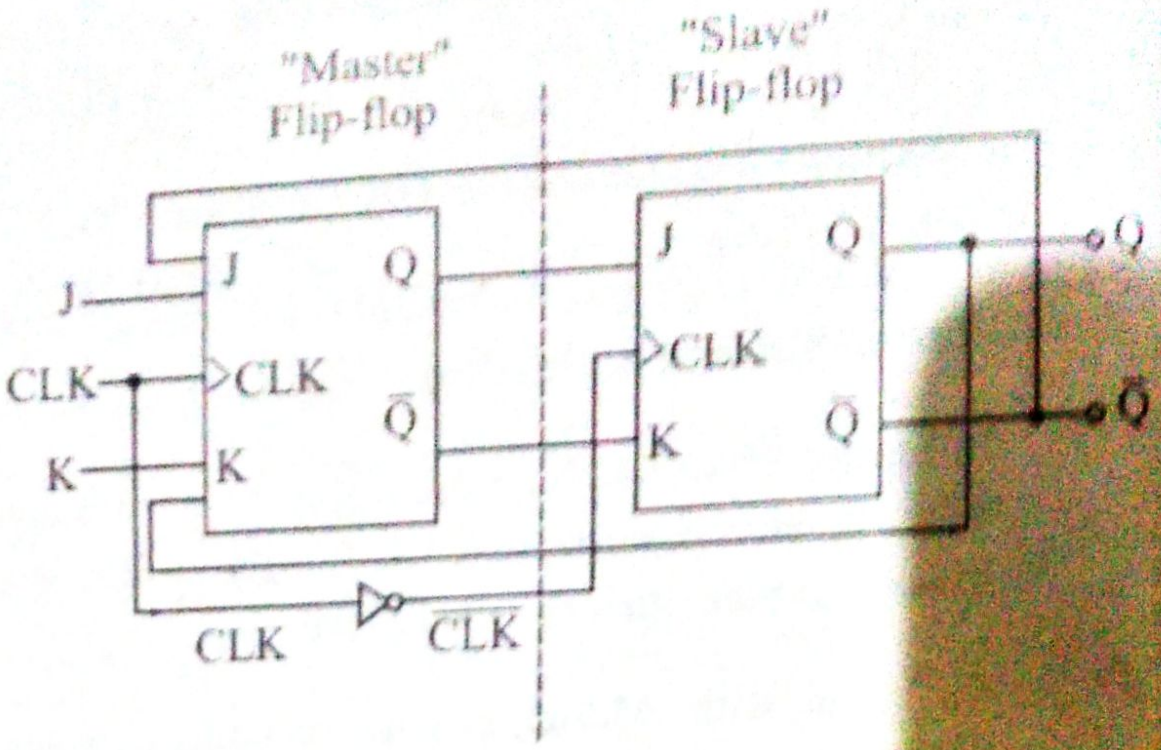
In Master Slave J-K flip flop, racing problem is avoided. This flip flop requires two J-K flip flops. One is called Master and the other is called Slave.

To begin with, Master is positive edge triggered and Slave is negative edge triggered. It means when Clk is high the master flip flop will respond to the inputs J and K and when Clk gets low, the slave flip flop will respond to output of master flip flop which are fed as input to the slave flip flop. The circuit diagram of master Slave J-K flip flop as follows:



(Master Slave J-K flip flop)

The logic diagram is as follows:



Working of master flip flop

The truth table of master flip flop is given below:

Inputs			Output	
CLK	J	K	Q_{n+1} (Q_1)	Description
1	0	0	Q_{n+1}	No change
1	1	0	1	Set
1	0	1	0	Reset
1	1	1	$\bar{Q}_n$	Toggle

When Clk = 1, master flip flop will work as follows:

- When J = 0 and K = 0 then the flip flop gets disabled. Hence there will be no change in the output.
- When J = 1 and K = 0, the master flip flop sets on the positive clock transition.

Q1.26 What is stable table?

Ans. ***A table which shows the inputs, outputs and flip flop state changes for sequential circuits is called state table.***

It consists of four sections, namely, present state, inputs, next state and outputs. The present state shows the state of flip flops before the occurrence of a clock pulse at any given time t. The next state shows the states of flip flops after the clock pulse at time t+1. Both the outputs and next state are a function of the inputs and the present state.

Q6.(a) Explain State Diagram. **MDU BCA 2018**

OR

What are State Diagrams? How are these relevant in design of Flip-Flops? Explain. **MDU BCA 2017**

OR

Discuss the concept of state diagram with examples. **MDU BCA 2016, 2015**

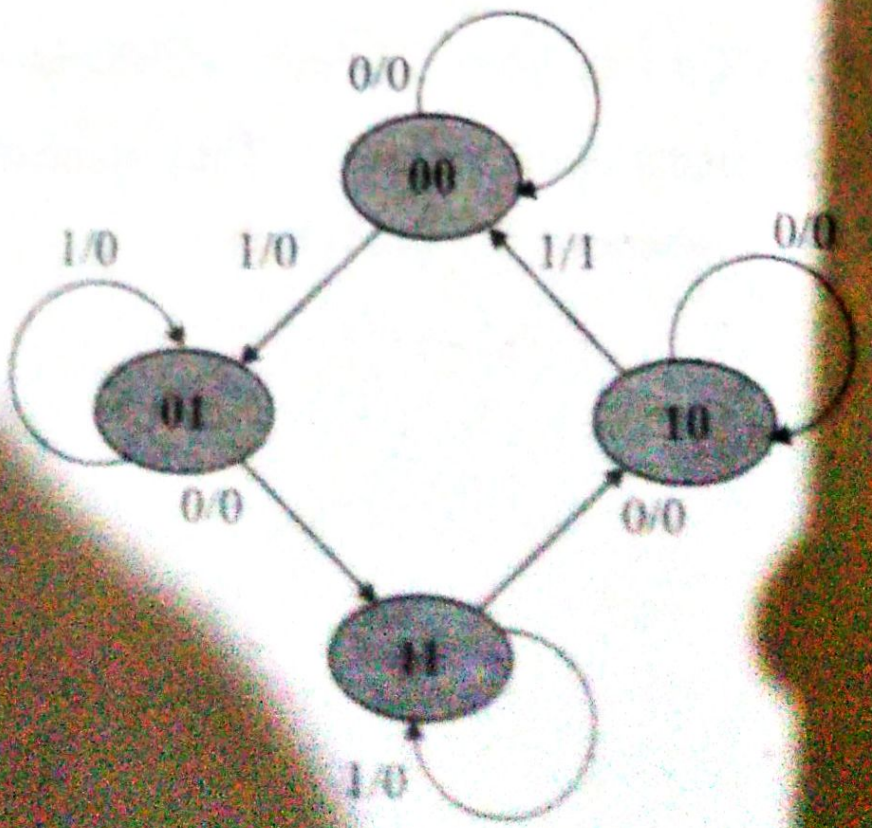
OR

Discuss state diagram. **MDU BCA 2014, 2013**

Ans. State diagram

A graphical representation of a state table is called a state diagram.

In state diagram, a state is represented by a circle, and the transition between states is indicated by directed lines (or arcs) connecting the circles. An example of a state diagram is shown is shown below:



The binary number inside each circle identifies the state the circle represents. The directed lines are labelled with two binary numbers separated by a slash (/). The input value that causes the state transition is labelled first. The number after the slash symbol / gives the value of the output. For example, the directed line from state 00 to 01 is labelled 1/0, meaning that, if the sequential circuit is in a present state and the input is 1, then the next state is 01 and the output is 0. If it is in a present state 00 and the input is 0, it will remain in that state. A directed line connecting a circle with itself indicates that no change of state occurs. The state diagram provides exactly the same information as the state table and is obtained directly from the state table.

specification.

Q1.26 What is stable table?

Ans. ***A table which shows the inputs, outputs and flip flop state changes for sequential circuits is called state table.***

It consists of four sections, namely, present state, inputs, next state and outputs. The present state shows the state of flip flops before the occurrence of a clock pulse at any given time t. The next state shows the states of flip flops after the clock pulse at time t+1. Both the outputs and next state are a function of the inputs and the present state.

Q5.(a) What are Excitation Tables? How are these relevant? Draw Excitation Table for RS and JK flip flop. MDU BCA 2018, 2017

OR

Give the excitation table for the following Flip-Flops:

(i) D Flip-Flop IGU BCA 2018

(ii) T Flip-Flop IGU BCA 2018

(iii) SR Flip-Flop IGU BCA 2018

OR

What are flip-flop excitation tables? Discuss with examples. MDU BCA 2016, 2015

Ans. Excitation table

During the design process, the transition from present state to next state is known. Now there is need to find the flip-flop input conditions that will cause the required transition. A table which lists the required inputs for a given chance of state is called an excitation table.

The required input conditions are derived from the information available in the Truth Table. The symbol ϕ in the table represents a "don't care" condition, i.e., it does not matter whether the input is 1 or 0. It is also sometimes denoted as X.

Thus, in the design of sequential circuits, it is often required to find input conditions so that desired next state of the circuit is obtained from the present state of the circuit. These input conditions can be obtained using

the excitation table of a flip flop. The truth table of a flip flop specifies its operational characteristic while the excitation table of a flip flop gives an idea regarding the present input conditions along with present state, to obtain the desired next state.

Excitation table for RS flip flop

Let the present state of the RS flip flop be $Q_n = 0$ and the desired next state be $Q_{n+1} = 0$.

As there is no change in the state of the flip flop (present state and next state is same), from the first row of the truth table of RS flip flop we obtain the input condition as S = 0 and R = 0.

Similarly from the third row of the truth table of RS flip flop, it is clear that whatever may be the present state, the next state of the flip flop is certainly 0 for the input condition S = 0 and R = 1.

By combining these two input conditions we conclude that S input must be 0 while R input can be 0 or 1, i.e., R input can be ϕ (don't care), to obtain the next state $Q_{n+1} = 0$ from the present state $Q_n = 0$. This gives first row of the excitation table of RS flip flop.

Similarly input conditions can be found for remaining three combinations of present state and next state. The excitation table is given below:

Q7.(a) Discuss Shift Register. **MDU BCA 2013**

OR

Define Shift Register. Explain various types of shift registers with their applications.

MDU BCA 2012

Ans. Shift Register

A shift register is a register which is capable of shifting the binary data in a register. They are a group of flip-flops connected in chain so that the output from one flip-flop becomes the input of the next flip-flop.

The information shifts from one flip-flop to the next as each new bit enters the register. Such type of register is commonly called shift register.

Thus shift register is a memory in which information is shifted one position at a time when one clock pulse is applied.

There are two ways to shift data in shift register. These are:

- ***In serial way***
- ***In parallel way***

In serial way, one bit at a time is shifted to a new place. In parallel way, all the bits are shifted simultaneously.

Data in a register can be shifted towards right (right shift register) or towards left (left shift register), depending upon the requirements.

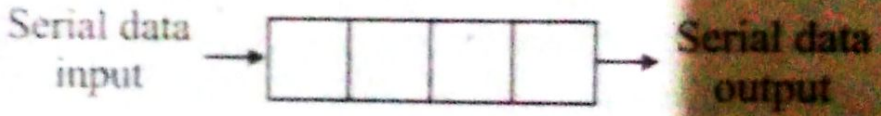
The storage capacity of a shift register is the number of bits of digital data it can retain.

The various shift registers are:

1. *Serial in, Serial out (SISO)*
2. *Serial in, Parallel out (SIPO)*
3. *Parallel in, Serial out (PISO)*
4. *Parallel in, Parallel out (PIPO)*

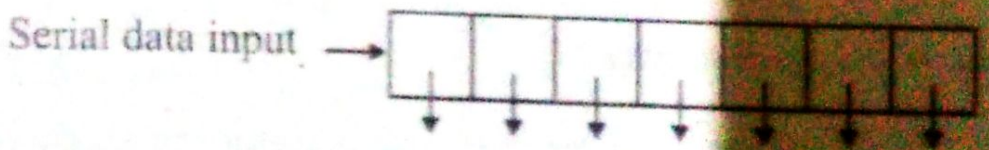
1. Serial in, Serial out (SISO) Shift Registers

These types of shift registers accept the data serially i.e. one bit at a time. It produces the stored information on its output also in serial form i.e. one bit at a time.



2. Serial in, Parallel out (SIPO) Shift Register

For serial in, parallel out shift register, data bits are entered serially i.e. one bit at a time. The stored information is taken out in parallel form i.e. all bits at a time.

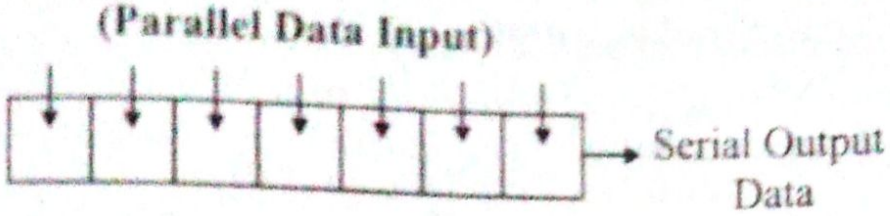


(Parallel Output)

3. Parallel in, Serial out (PISO) Shift Register

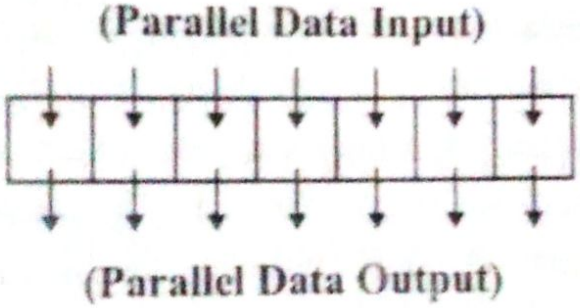
Parallel in serial out (PISO) work as reverse of serial in parallel out (SIPO). In PISO data entered parallel, i.e.,

all bits are stored simultaneously but data is taken out of register in a serial way like SISO register.



4. Parallel in, Parallel out (PIPO) Shift Register

Parallel in, parallel out shift register takes the data from the parallel inputs as in PISO register and take out in parallel way as in SIPO register.



Applications of Shift Registers

Shift registers are used in the following applications:

1. Serial to parallel data conversion

In many digital systems, serial data is used to reduce the number of input lines.

By using serial in, parallel out shift register, serial data can be converted to parallel data.

2. Parallel to serial data conversion

A parallel in serial out shift register can be used for conversion of parallel data to serial data.

3. Ring counters

Ring counters are constructed by modifying the serial in, serial out shift register. If the output of a shift register is fed back to serial input the shift register can be used as a ring counter. It is used to count the number of pulses.

4. Time delay

Serial in, serial out shift register can be used to introduce time delay from input to output. In some digital systems it becomes necessary to delay the transfer of data until such time as operation on other data have been completed or to synchronize the arrival of data at a subsystem. A shift register can be used to delay the arrival of serial data by a specific number of clock pulses.

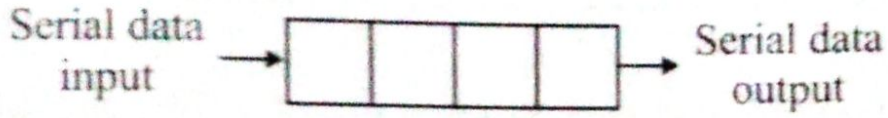
Q7.(b) Discuss Serial Input Serial Output.

MDU BCA 2013

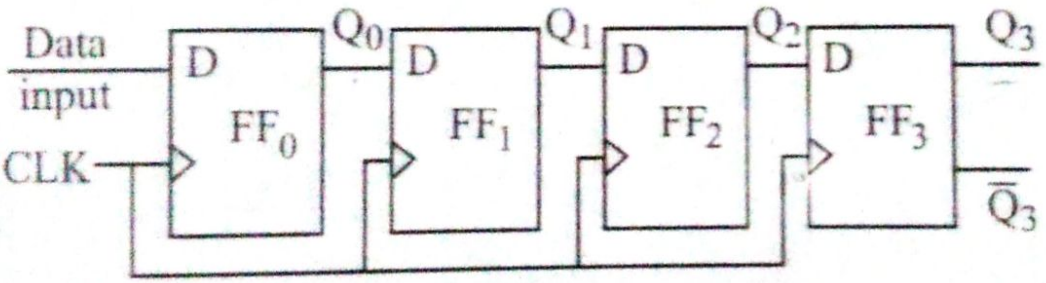
OR

Draw the circuit of serial in serial out shift register and explain its working.

Ans. These types of shift registers accept the data serially i.e. one bit at a time. It produces the stored information on its output also in serial form i.e. one bit at a time.



A basic four-bit shift register can be constructed using four D flip-flops as shown below:

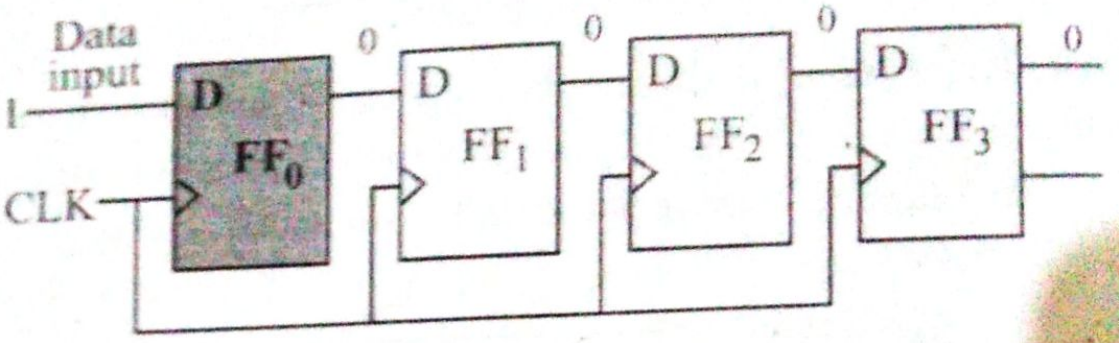


The operation of the circuit is as follows:

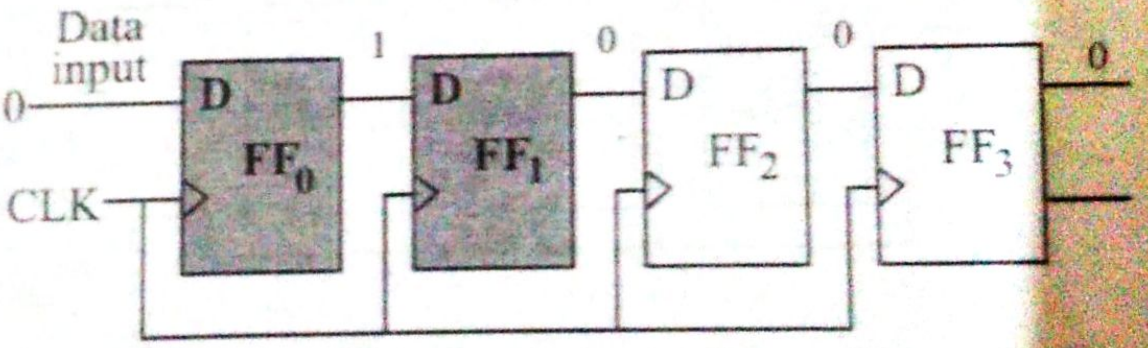
The register is first cleared, forcing all four outputs to zero. The input data is then applied sequentially to the D input of the first flip-flop on the left (FF_0).

During each clock pulse, one bit is transmitted from left to right. Assume a data word to be1001. The working of this register is:

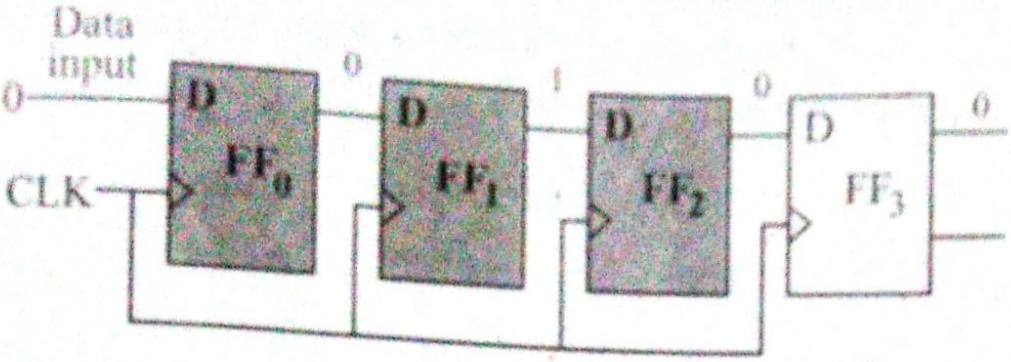
1. The least significant bit (LSB) i.e. the right most bit 1 is entered into the data input D=1 for FF_0. When the first clock pulse (CLK1) is applied FF_0 is SET and stores 1 as shown below:



2. Next bit 0 is entered i.e. 0 to D for FF_0 and 1 to D for FF_1 and second clock pulse is applied. This will shift 0 on the data input to FF_0 and 1 on data input to FF_1 as shown below:



3. Next bit 0 is entered and third clock pulse is applied. 0 is entered into FF_0, 0 stored in FF_0 is shifted to FF_1 and 1 stored in FF_1 is shifted to FF_2 as shown below:



4. Last bit 1 is entered and 4th clock pulse applied. 1 is entered into FF_0, 0 stored in FF_0 is shifted to FF_1, 0 stored in FF_1 is shifted to FF_2 and 1 stored in FF_2 is shifted to FF_3.

This completes the serial entity of 4 bit data into the register as shown below:

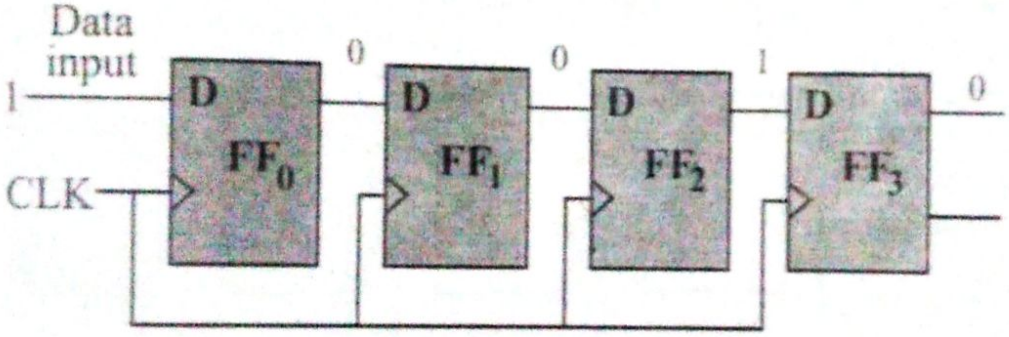
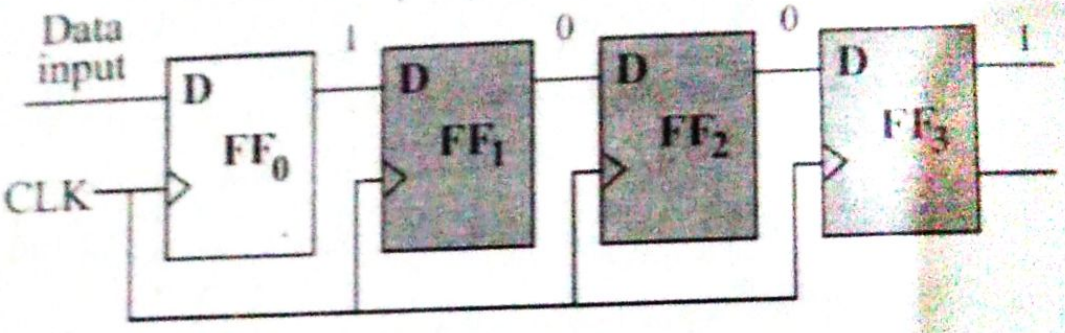


Table showing data transfer through serial input is:

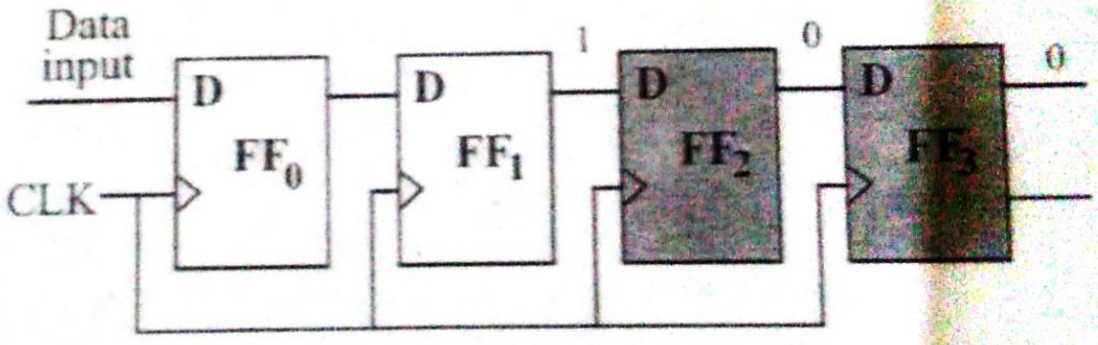
CLK	Date Input	FF_0	FF_1	FF_2	FF_3
0	1	0	0	0	0
1	0	1	0	0	0
2	0	0	1	0	0
3	1	0	0	1	0
4		1	0	0	1

In the same way, data can be taken out one bit at a time in a serial way as follows:

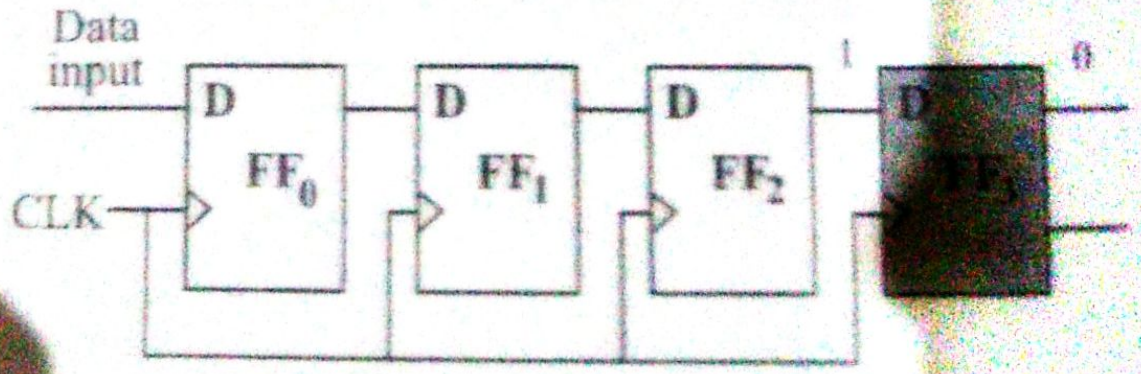
5. Clock pulse 5 is applied. Least significant bit (LSB) 1 is shifted out.



6. Clock pulse 6 is applied. The 0 on D for FF_3 is shifted out.



7. Clock pulse 7 is applied. The 0 on D for FF_3 is shifted out. 1 appears on D for FF_3.



Q7.(c) Design a 4-bit shift register and outline the procedure for serial to parallel conversion.

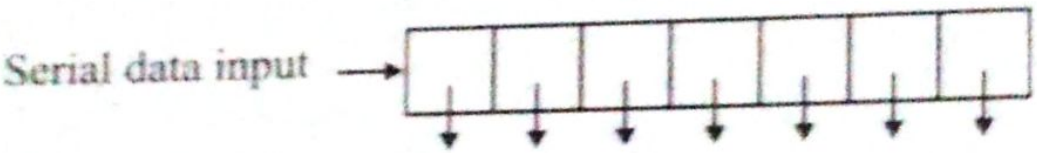
MDU BCA 2018, 2017

OR

Draw the circuit of a Serial in Parallel out Shift Register and explain its working.

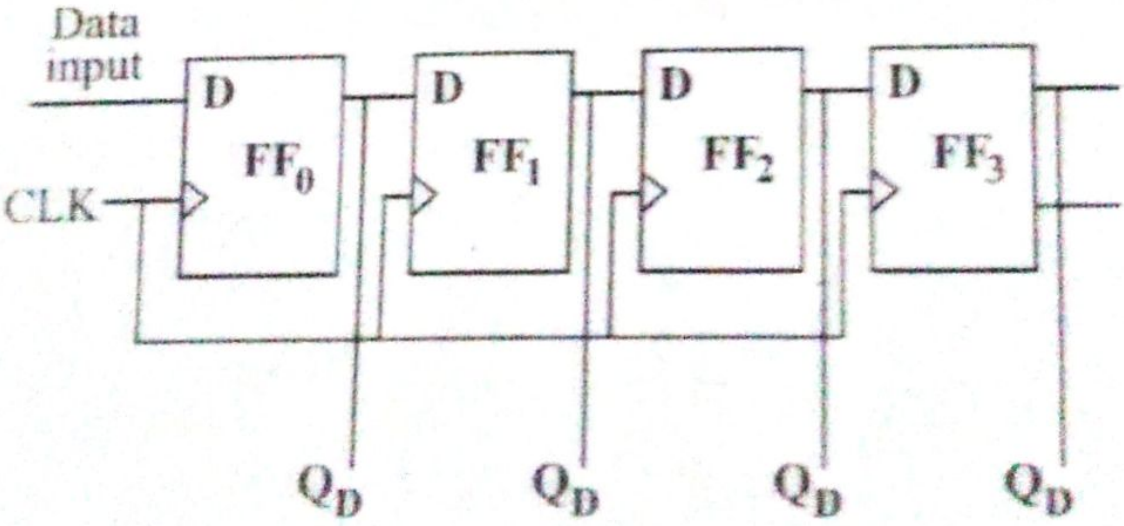
IGU BCA 2018

Ans. For serial in, parallel out shift register, data bits are entered serially i.e. one bit at a time. The stored information is taken out in parallel form i.e. all bits at a time.



(Parallel Output)

Figure shows four bit serial in parallel out shift register:



Thus the data entered into the register one bit at a time is same as in SISO register. Table shows four clock pulses to enter data 1001 into the SIPO register.

CLK	Date Input	FF_0	FF_1	FF_2	FF_3
0	1	0	0	0	0
1	0	1	0	0	0
2	0	0	1	0	0
3	1	0	0	1	0
4		1	0	0	1

To take data out of SIPO register, it will take only one clock pulse to take the data out as all the data is taken out simultaneously clearing all the flip flops. Thus after 5^{th} clock pulse:

FF_0	FF_1	FF_2	FF_3
1	0	0	1
↓	↓	↓	↓

All data is taken out concurrently.

Q8.(b) Draw the circuit of Parallel in Parallel out (PIPO) register and explain its working.

Ans. Parallel in, parallel out shift register takes the data from the parallel inputs A, B, C and D as in PISO register and take out in parallel way as in SIPO register.

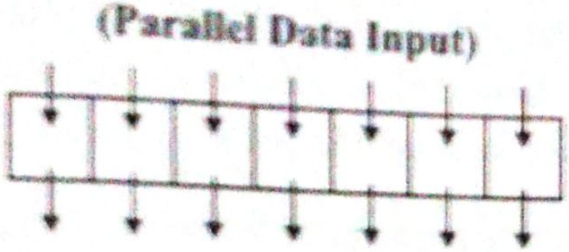
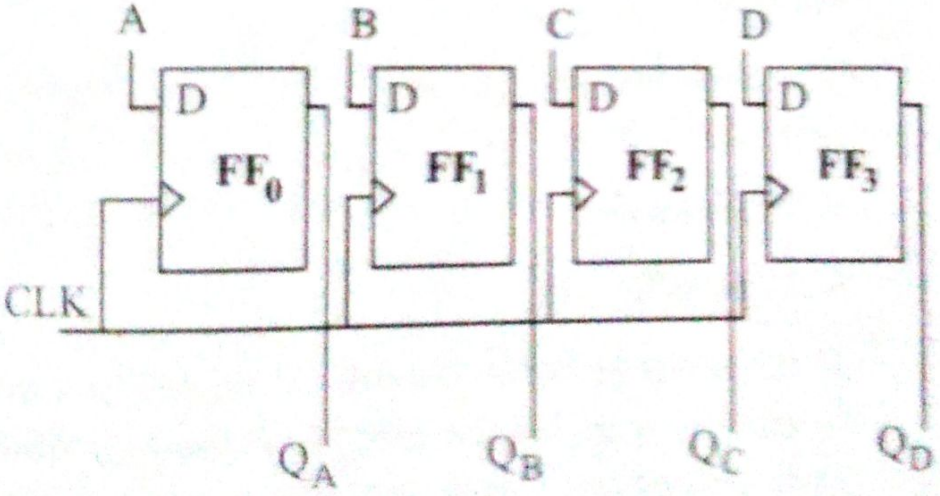


Figure shows a four bit parallel in parallel out (PIPO) shift register.



At one clock pulse the whole data word is shifted parallel to all the flip flops.

Thus at the end of one clock pulse, the data is stored in the register and similarly the data can be taken out in one clock pulse.

Q9.(a) Define counter. Describe the types of counters. Explain working of a synchronous counter with a suitable diagram. **MDU BCA 2012, 2011**

Ans. Counter

A counter can be defined as a register which is capable of counting the number of clock pulses in a digital system.

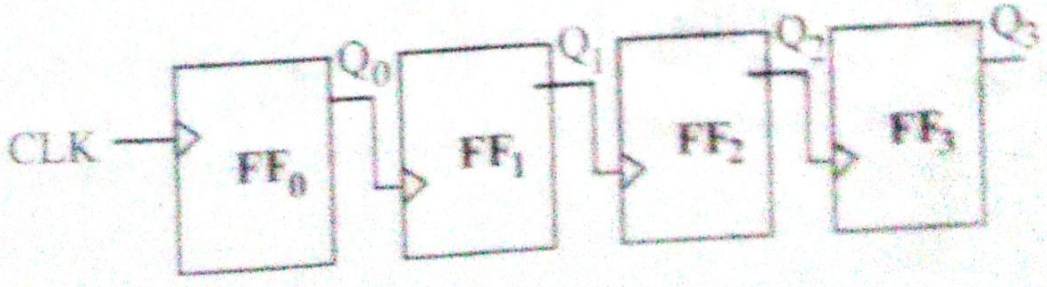
The counter has to actually count the number of clock pulses applied at the input. Counters are used in a variety of counting applications like control system, computers, electronic and scientific instruments etc.

Binary counters can be classified into two categories:

- ***Asynchronous Counters***
- ***Synchronous Counters***

Asynchronous Counters

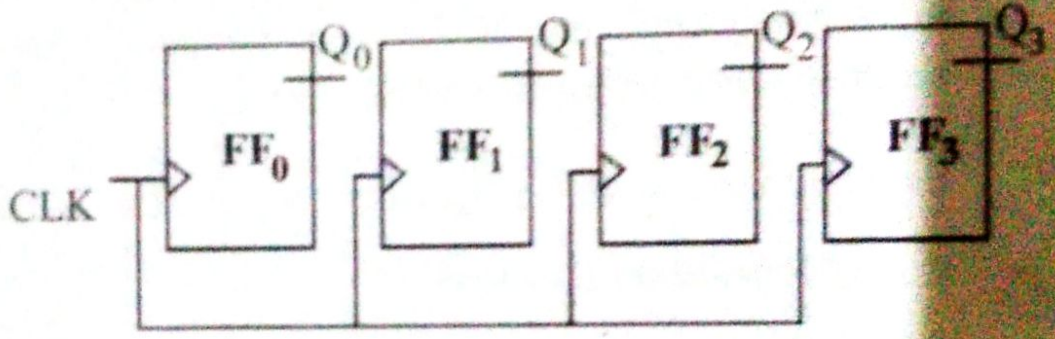
In asynchronous counter the clock pulses are not connected directly to clock input of each flip flop in the counter i.e. these counters do not work in synchronization with clock pulse. Here clock input is given to first flip flop and output of this flip flop becomes clock input for the second flip flop and so on.



An asynchronous counter is called as a ripple counter or modulo 2^n counter.

Synchronous Counters

Synchronous counter are those counters in which the clock input is connected to all the flip flops individually. It is clocked such that all the flip flops are clocked at the same time i.e. all flip flops work in synchronization with the clock pulse. They are used to increase the speed of operation.



Working of Synchronous Counters

A counter that counts from 0 to 9 is a mod-10 counter.

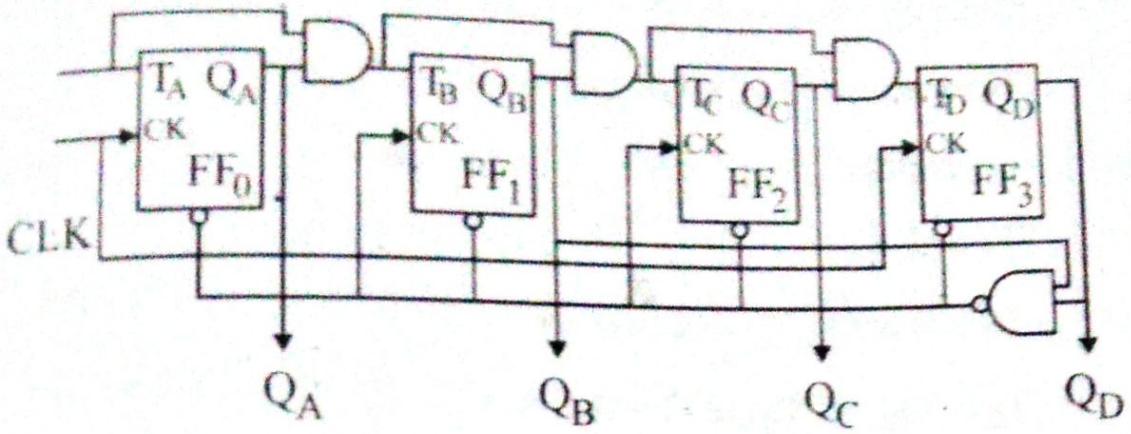
Number of flip flops required to design a counter is given by $2^n \geq k$.

Where n = Number of flip flops required.

k = Total number of states it can count.

Here $k = 10 \therefore n = 4$ since $2^4 = 16 > 10$

Figure shows mod-10 synchronous counter using T flip flop:



Counter Output

Truth table is:

Q_D	Q_C	Q_B	Q_A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

Working

Initially all flip flops are cleared making counter output

$Q_A\, Q_B\, Q_C\, Q_D = 0000$

Inputs of FFs are as follows:

$T_A = 1$

$T_B = 1 \times Q_A$

$T_C = Q_B \times T_B$

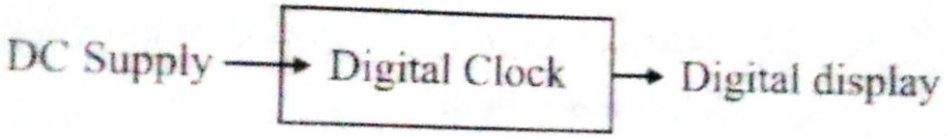
Q9.(b) Explain two applications of synchronous counter.

Ans. Synchronous counters have various applications in our daily life and engineering. Some of them are listed below:

1. Digital Clock

A counter is the main component of the digital clock.

- A digital clock uses the dc battery power supply of 60 Hz.
- The 60 Hz pulse is converted into hours, minutes and seconds.

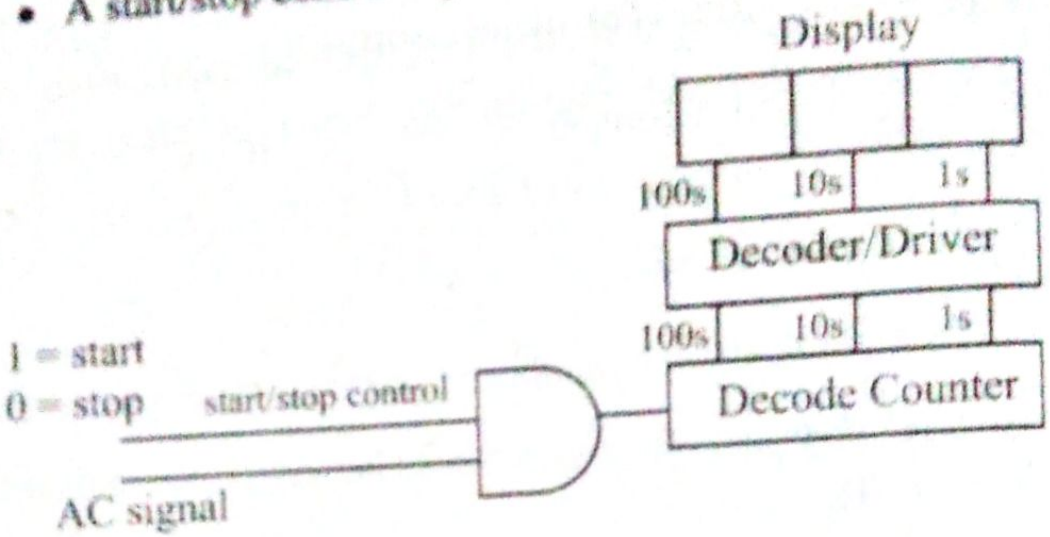


- Each pulse is divided by 60 counters and stored in the count accumulator for minutes and hours. The count is from 0 to 59.
- It is again reset to display the time in seconds.
- The stored contents of count accumulator are then decoded for display.

2. Digital Frequency Counter

- A digital frequency counter is used to measure the ac input signal.
- It also displays the frequency of ac input signal in digital form.

- The ac signal is fed to an AND gate.
- A start/stop control input is also fed to this AND gate.



- When start/stop control is at logical 1, the ac signal passes through the gate.
- The start/stop control at logical 0 stops ac signal from getting into the counter.
- The start/stop control is at logical 1 for 1 second and then returns to logical 0.
- The counter counts the number of pulses during this 1 second.
- The number is converted into decimal form and fed to display device.
- The display device displays the frequency.

3. LCD Timer with Alarm

- Many household applications like microwave ovens and washing machines etc. have a timer with alarm.
- These appliances use electronic timers and digital circuits.

Q10.(a) Explain up down counter.

MDU BCA 2018, 2013

Ans. Counter

A counter can be defined as a register which is capable of counting the number of clock pulses in a digital system.

The counter has to actually count the number of clock pulses applied at the input. Counters are used in a variety of counting applications like control system, computers, electronic and scientific instruments etc.

Binary counters can be classified into two categories:

- ***Asynchronous Counters***
- ***Synchronous Counters***

Asynchronous Counters

In asynchronous counter the clock pulses are not connected directly to clock input of each flip flop in the counter i.e. these counters do not work in synchronization with clock pulse. Here clock input is given to first flip flop and output of this flip flop becomes clock input for the second flip flop and so on.

Synchronous Counters

Synchronous counter are those counters in which the clock input is connected to all the flip flops individually. It is clocked such that all the flip flops are clocked at the same time i.e. all flip flops work in synchronization with

the clock pulse. They are used to increase the speed of operation.

Synchronous up/down Counter

- ***Synchronous up/down counter is a combination of J-K flip flops and NAND gates.***
- ***It can count in both downward and upward sequence/direction. It is also called bidirectional counter.***
- ***Up counter is a counter which can count in upward sequence.***
- ***A counter which can count in downward sequence is the down counter.***
- ***In up counter whenever clock pulse is applied, the count is always incremented by 1.***
- ***In down counter whenever clock pulse is applied, the count is always decremented by 1.***
- ***When clock pulse is applied, the 4 bit counter counts in the following way:***

Consider the diagram:

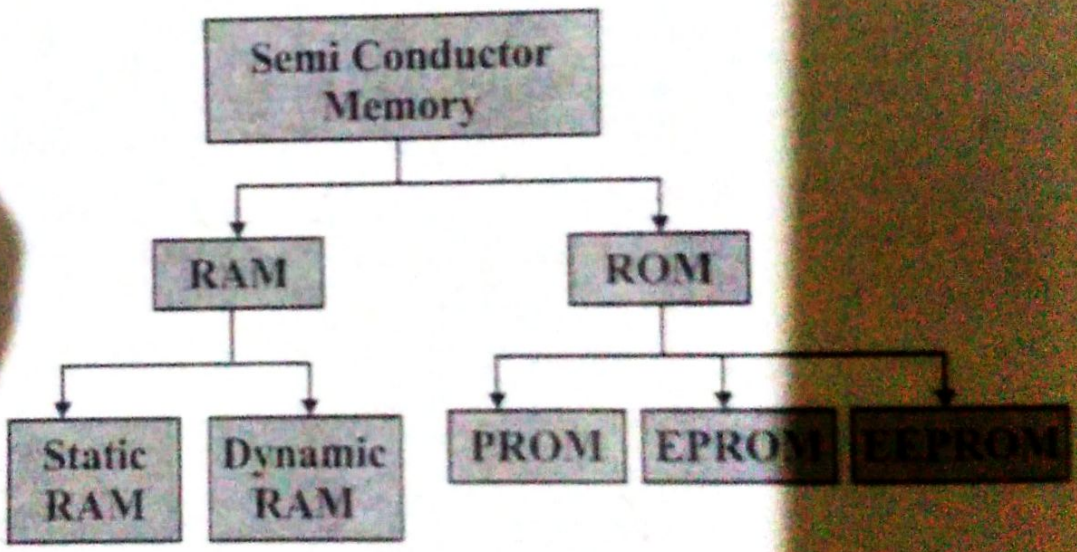
Q12.(a) Discuss different types of semiconductor memories. MDU BCA 2016, 2015

OR

What are various types of semi-conductor memories? State its types and applications.

Ans. Semi-conductor Memories

Semi-conductor memory was introduced in 1971 by IBM. This is faster and cheaper than magnetised core memory. All modern computers use this memory.



These memories use electronic circuit etched on silicon chip. The electronic circuit is called a flip-flop. The flip-flop circuits can store either 1 or 0. Millions of bits can be stored on a single chip and thus the physical size of the semi conductor memory is very small. With the use of chips, computers are now much more compact.

They consume lesser power and produce lesser heat. So too much cooling is not necessary. Because of integration, the pulses have to travel shorter distance and

the speed of operation of semiconductor memory is quite high.

These memories are of two types:

1. RAM (Random Access Memory).
2. ROM (Read Only Memory)

1. RAM (Random Access memory)

RAM is Random Access Memory as one can access any memory cell directly. It is the memory area where all data/ information get stored when a computer operates on a process. It stores data and applications currently in use.

The RAM is volatile in nature. The stored information is retained as long as the power supply is on. It loses its contents when power supply is switched off or interrupted.

RAM is of two types:

- Dynamic RAM (DRAM)
- Static RAM

Dynamic RAM (DRAM)

Dynamic RAM is the most commonly used computer memory. Inside a dynamic RAM chip, each memory cell holds one bit of information.

Each memory cell of Dynamic RAM is made up of one transistor and one capacitor. Capacitor is capable of storing electric charge. Transistor works as a switching device, which gives two states on and off. When

transistor is on, the charge on the capacitor indicates a '1' bit else no charge indicates a '0' bit.

The charge on the capacitor leaks away after a few milliseconds. Therefore, dynamic RAM has to be refreshed periodically after every two milliseconds. This process is called regeneration and since the process happens again and again, it is called dynamic RAM.

A dynamic RAM loses its contents in a very short time even though the power supply is on. Cost of these RAMs are less as compared to static RAM. They consume less power and have high packing density. These are recommended where large capacity of memory is needed.

Static RAM

Static RAM is also volatile in nature but needs no regenerator. They retain stored information as long as they receive the power and that is how static RAM gets its name.

In static RAM, a form of flip flop holds each bit of memory. They have higher speed than dynamic RAMs. They need more power and are more expensive. Static RAM circuit is more complicated and thus require more space. These are recommended where less capacity of memory is needed.

2. ROM (Read Only Memory)

It is a read only memory. It contains the information written into it during manufacturing. The information can only be read from the ROM. This memory is non-

volatile which means the information is not lost when the power goes off.

The ROM stores certain programs that are automatically loaded into the main memory when power is switched on. It is used to hold certain essential instructions in a computer.

Types of ROM

PROM (programmable Read only Memory)

PROM can be programmed after its manufacture to record data using a facility known as a prom-programmer. The contents are decided by the user. It can store data, programs or any other kind of information.

It can be programmed only once i.e. once the chip has been programmed the recorded information cannot be changed. In the PROM chip there are small fuses that can be programmed to a 1 or 0 by burning out a fusible link. A link once fused cannot be changed.

EPROM (Erasable Programmable Read only Memory)

EPROM can be erased by exposing it to ultra violet light for about 10 to 30 minutes. In this all the storage cells must be erased to the same initial state.

EPROM chip can be erased as many times as required. After erasing it can be reprogrammed using electrical impulses. EPROMs are widely used as they are cheap and reliable.

Q15.(a) **Explain Flash Memory.** MDU BCA 2018, 2013

OR

Write note on Flash Memory.

MDU BCA 2015, 2014

Ans. **Flash Memory**

Flash memory is a type of constantly powered nonvolatile memory that can be erased and reprogrammed in units of memory called blocks.

It is a form of semiconductor memory widely used for many electronics data storage applications. It is a form of non-volatile memory developed out of a combination of the traditional EPROM and EEPROM.

It uses the same method of programming as the standard EPROM and the eraser method of EEPROM. The difference is that EEPROM requires data to be written or erased one byte at a time whereas flash memory chip allows data to be written or erased in blocks. Thus, flash memory gets its name. Its microchip is organized in a way that a section of memory cells are erased in a single action or "in a flash".

Toshiba invented flash memory in 1980s as a new memory technology. Few examples of flash memory are:

- ***Computer's BIOS chip***
- ***Compact Flash often found in digital cameras***
- ***Smart Media found in digital camera***

- *Memory Stick found in digital camera*
- *PCMCIA Type I and Type II memory cards used in Laptops.*
- *Memory cards for video game consoles.*

Benefits and uses of Flash Memory

Following are the benefits and uses of Flash Memory:

- *It is a computer memory chip that maintains stored information without requiring a power source. It is useful in portable electronics such as digital music devices, smart phones, digital cameras and in removable storage devices.*
- *This technology is useful for computer basic input/output systems (BIOS), modems and video game cards.*
- *Flash memory has become so powerful, so fast and so large as far as volume is concerned that it is even used in some digital video cameras and as external portable hard drives.*
- *Flash memory is important and advantageous for data storage, retrieval and transfer.*
- *Flash memory can erase its data in entire blocks, making it a preferable technology for applications that require frequent updating of large amounts of data, as in the case of a memory stick for a digital electronic device.*

- *Flash memory allowed stored data to be saved even when the memory device was disconnected from its power source.*
- *Flash memory is widely used in notebook computers, tablets, digital cameras, Global Positioning Systems (GPS), Mobile phones etc.*
- *Flash memory is also used in many industrial applications where reliability and data retention in power-off situations are key requirements such as in security systems, military systems, embedded computers, solid state drives etc.*

Q16.(a) **Explain any four input and four output devices of a computer.** **IGU BCA 2018**

Ans. **Input Devices**

Devices, which are used to enter data & programs into the computer, are called input devices.

There are several input devices that are available today. Some of them are as follows:

- ***Keyboard***
- ***Mouse***
- ***Joystick***
- ***Trackball***
- ***Touch ball***
- ***Light Pen***
- ***Digitizers***
- ***Touch pad***
- ***Voice Recognition***
- ***Magnetic Ink Character Recognition (MICR)***
- ***Magnetic Strips***
- ***Optical Recognition***
- ***Point to Sale Terminal***
- ***Vision based devices***
- ***Data scanning devices***

There has been a great change in the input devices of the early computer age and today. Today a user can use any input device with a great ease whereas earlier the input devices were very complicated.

Input devices are divided into two categories: Text input devices and Cursor control devices. In text input devices the mainly used input device is keyboard. Cursor control devices are mouse, joystick etc.

1. Keyboard

Keyboard is an input device that converts alphabets, numbers and other special characters into electrical pulses which are understood by the computers. It is the most commonly and very popular input device of the present time. It is online device that is used for entering data directly into a computer.

Layout of keyboard is same as that of a typewriter. However the keyboard has certain additional keys like the function keys, arrow keys etc., which the typewriter does not have.

Through the keyboard only textual information can be entered. When a key is pressed, a signal is sent to the computer, which is decoded there to find out which key has been pressed.

The keyboard comes in a variety of sizes and shapes but most keyboards used with computer have the following five parts:

(i) Standard typewriter keys.

(a) Optical touch panel

Optical touch panel uses infrared light-emitting diodes and detectors around the edges of frame. These detectors will record those beams which are blocked when the panel is touched.

(b) Electrical touch panel

It uses conductive material to coat the plates. The plate is a basic component of Electrical touch panel.

(c) Acoustic touch panel

In acoustic touch panel high frequency sound waves are generated. When a point of screen is touched, then its location is identified by checking the time of gap between the wave transmission and its reflection to emitter.

Output devices

The processed information is communicated to the outside world through output devices.

Output devices can be classified into two types: Hard copy devices and Soft copy devices.

Hard copy devices are those devices that provide the output in permanent form. For example: Printers, Plotters etc.

In soft copy devices when power is switched off, information is lost. Information is on display till power is ON. Visual Display Unit comes under this category. A monitor is a visual display device.

Monitors

Monitors are the most popular output devices used for producing softcopy output. They display the processed results or output on a screen.

A monitor is a display device which can produce text and graphic as output. It is the most widely used output device.

Text output consists of alphabets, digits, and special characters. Graphics output includes images, drawings, charts, maps, photographs etc.

It is the major man-machine interface in computer system. It is used to display data or information. It allows the user to view the results of processing.

On the basis of operation, it is of two types:

(i) Cathode ray tube (CRT)

(ii) Flat Panel Display

(i) Cathode ray tube

The operations of most of the video monitor is based on the cathode ray tube CRT) technologies. CRT consists of a vacuum tube enclosed in glass. One end of the tube contains electron gun and the other end contains a screen with phosphorus coating. When heated, the electronic beam, emitted by heated electron gun, moves across a phosphor coated system. The phosphor coating glows at each position contacted by the electron beam and forms the characters.

Q17.(a) Explain the different phases of instruction cycle that is needed for the execution of an instruction used in addressing modes.

IGU BCA 2018

OR

Explain Instruction Cycle.

MDU BCA 2017, 2013, 2011

OR

What do you mean by an Instruction Cycle? What are various subcycles in an instruction cycle? Also outline the steps performed during each of these subcycles. **MDU BCA 2008**

Ans. Instruction Cycle

The instruction cycle is the time period during which one instruction is fetched from memory and executed when a computer is given an instruction in machine language.

A program is a sequence of instructions. To execute these instructions a group of steps are followed. Each instruction passes through some specific phase to complete its execution. A complete cycle used to execute one instruction is called fetch execute cycle or instruction cycle or machine cycle.

Subcycles in an instruction

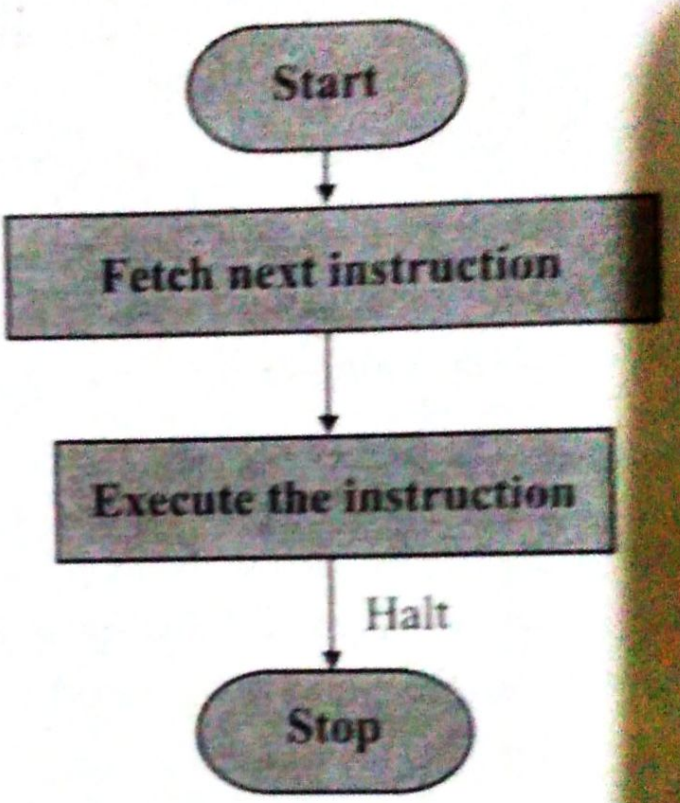
There are four stages of an instruction cycle that the CPU carries out. These are:

1. ***Fetch the instruction from main memory.***
2. ***Decode the instruction.***

3. *Read the effective address from memory of the instruction which has an indirect address.*

4. *Execute the instruction.*

Step1 and 2 are called the fetch cycle and are the same for each instruction. Steps 3 and 4 are called the execute cycle and will change with each instruction.



Thus the instruction cycle comprises of two subcycles – fetch cycle and execute cycle.

Fetch Cycle

When a program is executed:

- *The control unit issues the control signal to fetch the first instruction as indicated by the program counter (PC).*
- *This instruction is fetched to instruction register (IR).*

- *Program counter (PC) is incremented to get the location of next instruction.*
- *In the next step, the instruction is decoded which means operator and operands are separated, then address of the operand is calculated.*
- *The address of operands is placed in memory address register (MAR).*
- *Now the control unit issues a control read signal to read the data from the main memory, the location is stored in MAR.*
- *The data or operand value is transferred in the accumulator register.*
- *Now the fetch phase is over and the next execution cycle starts.*

Execution Cycle

Once an instruction has been fetched and decoded, the instruction execution cycle begins.

- *All the jobs are made ready for this phase during fetch phase. The only left work is to perform the defined operation on the operands.*
- *Thus the instruction is executed and result of this instruction is placed in MBR.*
- *The control unit, on completion of execution, issues the control write signal and the address of result data is placed on address bus in order to send and store the result at the appropriate place.*

Q19.(a) What are Addressing Modes? What are different Addressing Modes? Illustrate through examples. **MDU BCA 2018**

OR

What are addressing modes? Why it is used? Explain various addressing modes that are used in computers. **MDU BCA 2014**

OR

What are addressing modes? What are its various types? Indicate the significance and suitability of each of these addressing modes along with example of each. **MDU BCA 2013**

OR

Explain addressing modes with examples. **MDU BCA 2011**

Ans. Addressing Modes

Each instruction of a computer specifies an operation on certain data. There are various ways of specifying address of the data to be operated on. These different ways of specifying data are called the addressing modes.

Addressing mode is defined as a way or technique of determining the address of the operands in the memory.

An instruction contains operation code and operands. An operand may be part of an instruction, or the reference of memory location where the value is stored. The addressing modes describe the types of operands and the way they are accessed for executing an instruction.

PC register contains the address of the instruction to be executed and is incremented each time an instruction is fetched from memory.

Why addressing modes are used?

Addressing modes are used:

- ***To reduce storage required by programs***
- ***To reduce the execution time of programs.***
- ***To address data and instructions.***

Types of addressing modes

Various types of addressing modes are:

1. Immediate addressing
2. Direct addressing
3. Indirect addressing
4. Register addressing
5. Register indirect addressing
6. Displacement addressing
7. Stack addressing

1. Immediate addressing

In immediate addressing, the operand is specified in the instruction itself i.e. the operand field contains the actual operand to be used.

Instruction

Opmode	Operand

This mode is used for initialization of registers or memory variables.

For example: ADD 10

Adds 10 to contents of accumulator, 10 is operand.

Thus in immediate addressing mode:

- ***Operand is part of instruction.***
- ***The main advantage is that there is no memory reference to fetch data.***
- ***The main disadvantage is limited operand magnitude.***

2. Direct addressing

In direct addressing, the address field contains the effective address of the operand.

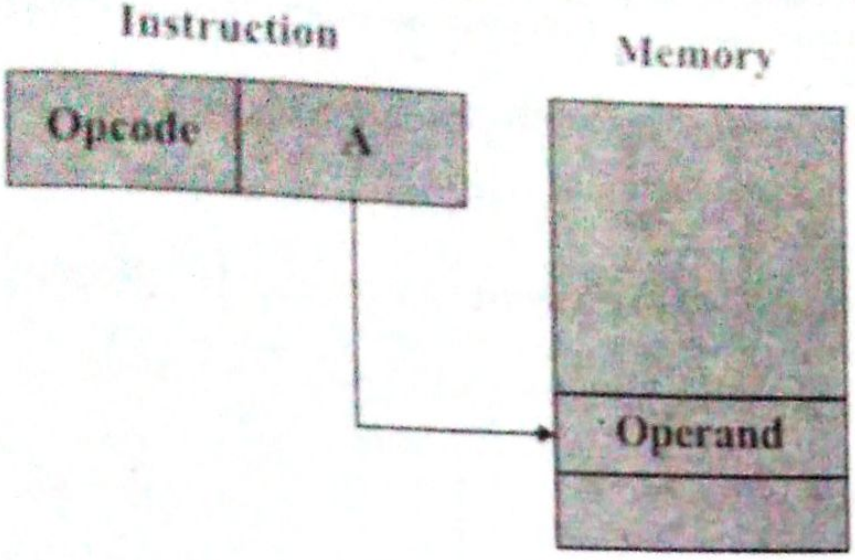
i.e. EA = A

Where: EA is effective (actual) address of the location containing the referenced operand.

A contains the contents of an address field in the instruction.

e. g. ADD A

Adds contents of cell A to accumulator, it looks in memory at address A for operand.



Thus in direct addressing mode:

- ***Operand resides in memory and its address is given directly in the address field of the instruction.***
- ***It requires only one memory reference to access data.***
- ***No additional calculations to work out effective address.***
- ***The main disadvantage is its limited address space.***

3. Indirect addressing

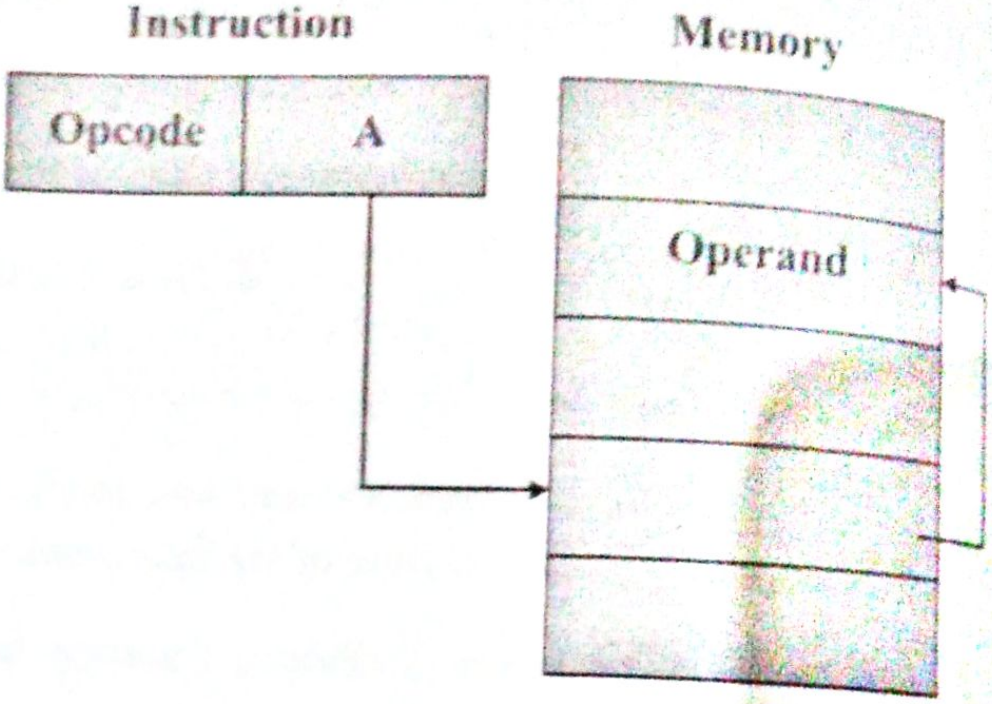
In indirect addressing, the address field contains the address of a word in memory which in turn contains the address of the operand.

i.e. EA = (A)

Looks in A, find address (A) and look there for operand. Here the parentheses are to be interpreted as meaning contents of.

e.g. ADD (A)

Adds contents of cell pointed to be contents of A to accumulator.



Thus in indirect addressing mode:

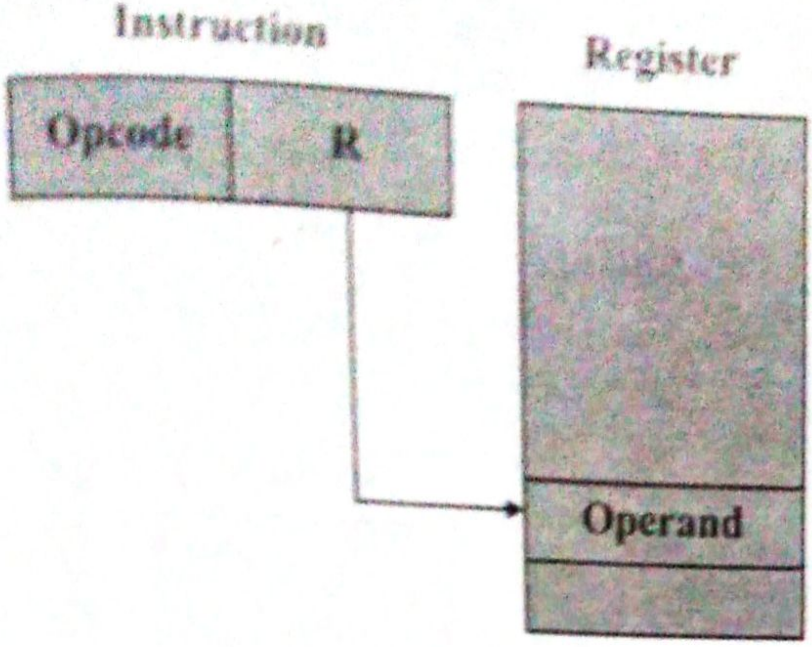
- ***Address field points to memory cell which contains the address of the operand.***
- ***Address space is large.***
- ***The main disadvantage is that it requires two memory references to fetch the operand, one to get its address and second to get its value. Thus it is slow.***

4. Register addressing

In register addressing, the instruction specifies the address of register containing the operand. It is like direct addressing, the only difference is that the address field refers to a register instead of memory address.

i.e., EA = R

Where EA is effective (actual) address of the location containing the referenced operand. R is register.



e.g. MOV B, A

It moves the contents of the accumulator register A to the general purpose B register.

Thus in register addressing mode:

- ***Operand is held in register named in address field.***
- ***Only a few bits are required to address the operand.***
- ***No memory references are required.***
- ***Very fast execution.***
- ***The disadvantage is very limited address space.***

5. Register indirect addressing

In register indirect addressing, the instruction specifies a register in the CPU whose contents give the address of operand in memory.

Q19.(b) Write short note on Input Output Interface.

IGU BCA 2018

OR

What do you understand by Input/Output Interfacing? State its types as well as the importance of each type of interfacing.

MDU BCA 2012, 2011

Ans. Input/Output Interface

I/O devices establish communication of computer with the outside world. Whenever the communication is to be done between I/O devices and microprocessor it needs an interface. Such interface is called Input/Output interface.

The I/O interface supervises and synchronizes all input and output transfers between internal storage and external I/O devices.

I/O interfacing is of two types:

1. I/O mapped I/O

This type is also known as isolated input/output. Here input or output device/port is treated separate from memory location. So this method of input/output isolates memory and I/O addresses.

Features of I/O mapped I/O

Following are the features of I/O mapped I/O:

- ***Each device is identified with a unique device number.***

- *In the isolated I/O, the CPU has distinct input and output instructions.*
- *Only 16-address lines are used to address I/O devices.*
- *Data are transferred through IN/OUT instructions.*
- *IN instruction accepts input data from an input device and stores it in accumulator.*
- *OUT instruction sends output data from accumulator to output device.*

Importance of I/O mapped I/O

Following is the importance of I/O mapped I/O:

- *Less hardware is required to decode an address.*
- *Memory space is not lost.*
- *This scheme is suitable for a large system.*

2. Memory mapped I/O

In a memory mapped I/O organization, I/O devices are considered as part of memory. Since I/O device is treated as a memory location, the communication between the microprocessor and I/O devices is like communication of microprocessor and memory.

Features of memory mapped I/O

Following are the features of memory mapped I/O:

- *There is no specific input or output instructions.*

- *Memory type instructions can be used to access I/O data.*
- *I/O ports are connected with microprocessor with 16-bit address assigned to each port.*
- *The control signals used are* $\overline{\text{MRD}}$ *for input port and* $\overline{\text{MWR}}$ *for output port.*
- *The instructions used for data transfer are LDA, STA, LDAX, PUSH etc.*

Importance of memory mapped I/O

1. Capacity expansion

In the microprocessor based applications sometimes a single memory chip can not provide the required capacity. So by interconnecting various memory devices to each other, required capacity is achieved.

2. Increased utilization

All applications do not require complete address space. The memory devices can be contiguously placed and hence complete address space of microprocessor can be utilized.

3. Ease in data transfer

Data transfer with any register is easier to make.

4. Suitability

Memory mapped input output scheme is suitable for a small system.

Q20.(a) What are interrupts? How are these useful? Illustrate. **MDU BCA 2017**

OR

What is Interrupt? What is the role of interrupt in the operation of a computer system? **MDU BCA 2010**

Ans. Interrupt

An interrupt is an event that causes the execution of one program to be suspended and another program is executed.

In computing, an interrupt is an asynchronous signal indicating the need for attention or a synchronous event in software indicating the need for a change in execution.

Interrupt can also be defined as externally triggered event that makes a computer halt current processing and initiate a new sequence of instructions.

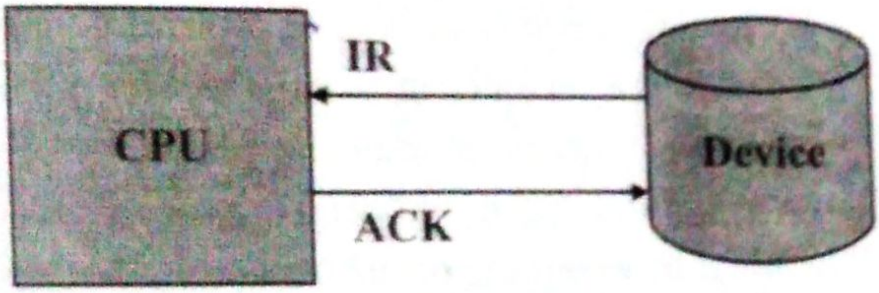
Interrupts are often used in I/O operations by a device interface or controller to notify the CPU that it has completed an I/O operation.

An interrupt signal is sent by a peripheral device to the CPU when it is ready to send or receive information to or from the memory.

When an interrupt signal arrives, CPU follows the following steps:

- ***CPU receives a signal, known as interrupt request (IR).***

- *CPU completes its current instruction.*
- *Value of program counter (PC) and other general purpose registers is saved in memory by the CPU.*
- *CPU sends an acknowledgmemt signal to the device and takes up an interrupt service routine.*
- *The transfer of information from or to the peripheral device takes place.*
- *After the interrupt is serviced, this state information is restored.*
- *Program counter is set again and CPU resumes its original working.*



Types of Interrupt

CPU handles several interrupts from I/O programs or devices. Following are the three types of interrupts:

1. External Interrupts
2. Internal Interrupts
3. Software Interrupts

1. External Interrupts

External interrupts are the interrupts caused by either of:

- *I/O devices.*

- *Emergency events outside the CPU's control such as sensing of power failure.*

2. Internal Interrupts

Internal interrupts are the interrupts caused by a user's program due to illegal use of an instruction or data. In case of some mistakes like divide by zero, stack overflow or use of a wrong operation code, the CPU interrupts the userprogram, suspends its execution and takes appropriate steps and then resumes its normal execution.

3. Software Interrupts

Software interrupts are usually caused by instructions in the instruction set. It is a special call instruction that behaves like an interrupt. This type of interrupts occur when user initiates an interrupt procedure at any point in the program. Such interrupts may be many and are handled by assigning priorities to all interrupts.

Usefulness of interrupts/Role of interrupt in the operation of a computer system

In addition to controlling I/O transfers, interrupts play a significant role in the following ways:

1. Helps recover from errors

Computers use many techniques to ensure proper operation. In case an error occurs, the control hardware informs the CPU by raising an interrupt. The CPU may also interrupt a program if it detects an error or unusual condition while execution of a program. In such cases,

when an interrupt is initiated, CPU suspends the executing program and starts an interrupt service routine. This routine either takes appropriate action to recover from the error or informs the user about it.

2. Aid in Debugging

A debugger program in the system software helps the programmer to find errors in the program. The debugger uses interrupts for two purposes:

- Trace
- Break

For a trace facility, an interrupt occurs after execution of every instruction of program being debugged. On a trace interrupt, the interrupt service routine starts the execution of the debugging routine which helps the user to examine the contents of registers and memory locations etc.

To provide break facility, the program being debugged is interrupted at only specific points selected by the user. An instruction called trap or software interrupt is used for this purpose. For example if the user plans to interrupt a program after execution of the ith instruction, the debugging routine replaces (i+1)th instruction with a software interrupt instruction.

3. Communication between Programs

Operating system also uses software interrupt instructions to communicate with other programs and also control the execution of other programs.

Q20.(c) Explain the program controlled and interrupt controlled data transfer.

Ans. Program controlled data transfer

Program controlled I/O is a way of moving data between devices in a computer in which all data must pass through the CPU. In this data transfer scheme, a software program residing in memory request the device for data transfer to or from the CPU.

The Accumlator and other CPU registers are involved in data transfer.

Using this strategy, the CPU is responsible for all communications with I/O modules by executing instructions which control the attached devices or transfer data.

While executing a program, CPU encounters an instruction relating to I/O. CPU executes the instruction by issuing a command to the appropriate I/O module. Then the I/O module performs the request action and sets the appropriate bits in the I/O status register.

Q21.(b) Is programmed I/O technique not suitable for voluminous data transfer? If not, then illustrate the suitable technique for this purpose through its block diagram.

MDU BCA 2012

What do you mean by Direct Memory Access (DMA)? Why does DMA have priority over the CPU when both are used for memory transfer?

MDU BCA 2010

Ans. DMA

Programmed I/O is not suitable for voluminous data transfer, this is because all data is transmitted between peripheral devices goes through the CPU. A lot of CPU time is wasted in checking whether the I/O unit is ready for data transfer or not. So this results in poor CPU utilization. DMA (Direct Memory Access) technique is most suitable for heavy data transfer.

Direct memory access is a technique in which I/O device may transfer the data directly to/from memory without any interference from the CPU. Thus DMA means memory can be directly accessed by I/O devices keeping CPU free.

DMA technique can also be defined as that transfer technique in which peripheral devices directly manage the memory buses to speed up transfer by removing CPU from the path.

DMA uses an additional piece of hardware – a DMA controller. The DMA controller can take over the system

bus and transfer data between an I/O module and main memory without the intervention of the CPU.

Whenever CPU needs to transfer data, it informs the DMA controller:

- ***the direction of the transfer,***
- ***the I/O module involved,***
- ***the location of the data and memory and***
- ***the size of the block of data to be transferred.***

It can then continue with other instructions and the DMA controller interrupts it when the transfer is complete.

This technique allows data to be transferred between memory and I/O device at a rate that is limited only by the speed of the memory components in the system or the DMA controller.

Components of DMA Interface Unit

DMA interface unit should have following components.

1. Memory Address Register (MAR)

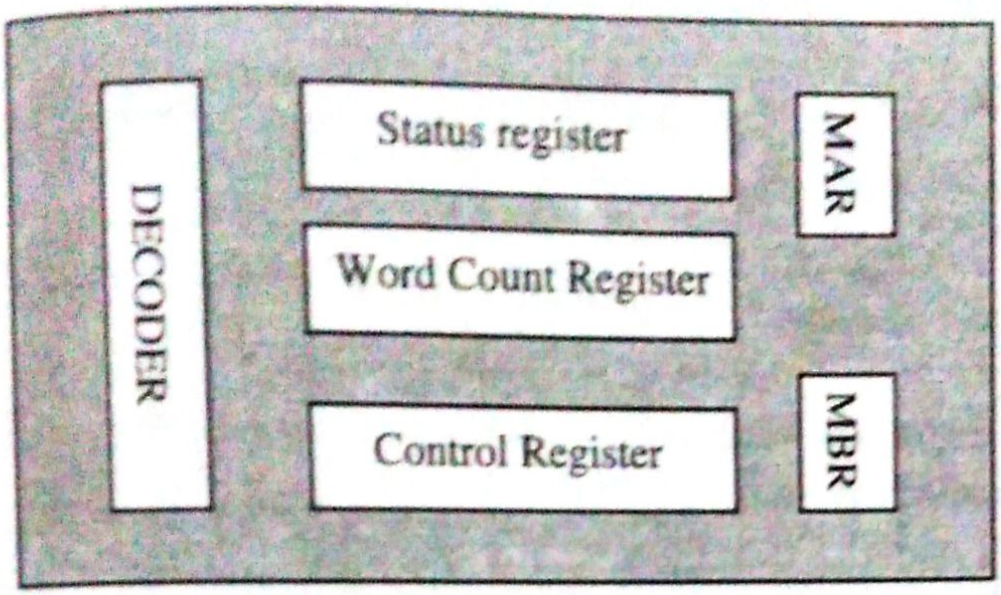
The memory address register contains an address to specify the location in memory from where data is received or data is to be transferred.

2. Memory Buffer Register (MBR)

This register contains the word to be sent to the memory or that received from memory.

3. Word Count Register

It holds the number of words to be transferred. This register is decremented by one after each word transfer and internally tested for zero.



4. Status Register

The status register is used to specify DMA busy/free, data ready and other status information.

5. Control Register

It specifies the modes of transfer like read or write.

6. Decoder

The address decoder decodes the address of the I/O device.

Working of DMA

The process of DMA mode takes place in the following sequence:

1. *An I/O request is issued.*
2. *CPU intercepts it and interprets it.*
3. *CPU sends signal to DMA. It includes device address, number of words to be transferred, address of first word to be transferred and the command.*
4. *After this the CPU is free and can be used for any other operation.*
5. *DMA starts working, decodes address, starts filling MBR, sets and resets the SR and DR.*
6. *Till MBR is filled, DMA will not entertain any other request.*
7. *When MBR is filled, data is transferred – address via Address Bus and data by Data Bus.*